REMARKS

The following Remarks are made in response to the Non-Final Office Action mailed May 2, 2006, in which claims 1-44 were rejected. The pending claims have not been amended. Claims 1-44, therefore, remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102 and 35 U.S.C. § 103

Claims 1, 2, 4-8, 10-18, 24-26, 33-44 are rejected under 35 U.S.C. 102(b) as being anticipated by the Axtell et al. US Patent Application No. 2002/0093551.

Claims 19-21 and 27-31 are rejected under 35 U.S.C. 102(b) as being anticipate by the Donahue et al. US Patent no. 6,174,037.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Axtell et al. US Patent Application No. 2002/0093551 in view of the Matsumoto et al. US Patent No. 5,057,885.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Axtell et al. US Patent Application No. 2002/0093551 in view of the Donahue et al. US Patent No. 6,174,037.

Claims 22, 23 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Donahue et al. US Patent No. 6,174,037 in view of the Axtell et al. US Patent Application No. 2002/0093551.

Applicant respectfully submits that the Axtell et al. Patent Application and the Donahue et al. Patent illustrate and describe circuit schematics. In the Axtell et al. Patent Application and the Donahue et al. Patent, elements in the circuit schematics are represented by schematic symbols of devices, such as transistors and resistors. The Axtell et al. Patent Application and Donahue et al. Patent circuit schematics do not illustrate physical structures of the construction of the elements as claimed in independent claims 1, 19, 24, 27, 33, 36, and 38. Example embodiments of physical structures claimed in the Present Application are illustrated in Figures 15A-19 and described in Present Specification at pages 76-91.

For example, in independent claim 1 structures not taught or suggested by the Axtell et al. Patent Application include: "a first transistor having a first gate configured in a first loop structure; a second transistor having a second gate configured in a second loop structure;

and a third transistor having a third gate configured in a third loop structure disposed around the first transistor, wherein the second transistor and the third transistor share a first active region."

Also, in independent claim 19 structures not taught or suggested by the Donahue et al. Patent include: "a first transistor having a first gate configured in a first loop structure; a second transistor having a second gate configured in a second loop structure; and a third transistor having a third gate configured in a third loop structure, wherein the first transistor and the second transistor are disposed within the third gate."

In independent claim 24 structures not taught or suggested by the Axtell et al. Patent Application include: "a substrate having a first active region and a second active region; a first gate configured in a first loop structure around the first active region; a second gate configured in a second loop structure around the second active region; and a third gate configured in a third loop structure around the first gate and the second gate."

In independent claim 27 structures not taught or suggested by the Donahue et al. Patent include: "a first transistor having a first gate configured in a first loop structure; a second transistor having a second gate configured in a second loop structure; a third transistor having a third gate configured in a third loop structure; and a fourth transistor having a fourth gate configured in a fourth loop structure, wherein the first transistor is disposed within the second gate and the third transistor is disposed within the fourth gate."

In independent claim 33 structures not taught or suggested by the Axtell et al. Patent Application include: "a substrate having a first active region, a second active region and a third active region; a first gate configured in a first loop structure around the first active region; a second gate configured in a second loop structure around the second active region; and a third gate configured in a third loop structure around the third active region."

In independent claim 36 structures not taught or suggested by the Axtell et al. Patent Application include: "a first transistor having a first gate, a first active region and a second active region, wherein the first gate is configured in a first loop structure around the first active region; and a second transistor having a second gate configured in a second loop structure around the second active region."

In independent claim 38 structures not taught or suggested by the Axtell et al. Patent Application include: "controlling a drive switch with a first transistor having a first gate

configured in a first loop structure, a second transistor having a second gate configured in a second loop structure, and a third transistor having a third gate configured in a third loop structure disposed around the first transistor, wherein the second transistor and the third transistor share a first active region."

In view of the above, Applicant respectfully submits that all features of independent claim 1, all features of independent claim 19, all features of independent claim 24, all features of independent claim 27, all features of independent claim 33, all features of independent claim 36, and all features of independent claim 38 are not taught or suggested by the Axtell et al. Patent or the Donahue et al. Patent alone or in combination with each other or other references of record.

Dependent claims 2-18 further define patentably distinct independent claim 1. Dependent claims 20-23 further define patentably distinct independent claim 19. Dependent claims 25 and 26 further define patentably distinct independent claim 24. Dependent claims 28-32 further define patentably distinct independent claim 27. Dependent claims 34 and 35 further define patentably distinct independent claim 33. Dependent claim 37 further defines patentably distinct independent claim 36. Dependent claims 39-44 further define patentably distinct independent claim 38. Accordingly, dependent claims 2-18, 20-23, 25, 26, 28-32, 34, 35, 37, and 39-44 are also believed to be allowable.

Therefore, Applicant respectfully requests that the above rejections under 35 U.S.C. § 102 and § 103 be withdrawn and that claims 1-44 be allowed.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-44 are all in a condition for allowance and requests reconsideration of the application and allowance of all pending claims.

The Examiner is invited to contact the Applicants' representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either James R. McDaniel at Telephone No. (858) 655-4157, Facsimile No. (858) 655-5859 or Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (571) 273-8300 on this 31 day of July, 2006.

By
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